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APPLIED PHYSICS LETTERS 105, 223506 (2014)

Scaling junctionless multigate field-effect transistors by step-doping

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Conventional junctionless (JL) multigate field-effect transistors (MuGFETs) use extremely scaled and highly doped fins as channels. Such small fins introduce large parasitic resistance as well as performance fluctuation due to fin width variations. The high channel doping significantly reduces bulk carrier mobility, which reduces on-state current and escalates short channel effect related leakage. In this letter, we present a step-doping scheme for the scaling of JL MuGFETs. By employing a two-step-doping profile, with the high doping side near the gate, higher threshold voltage and better off-state performance can be achieved, along with higher on-state current. This opens a route for threshold voltage design and addresses the design optimization for both on-state current and off-state leakage for JL MuGFETs. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4902864]

Junctionless (JL) multigate field-effect transistors (MuGFETs) have been proposed[1] as a potentially better alternative to traditional inversion mode MOSFETs for its scalability and fabrication simplicity.[2,3] Conventional JL MuGFET design involves a uniformly doped channel at a high level (typically $N_D > 10^{19}\,cm^{-3}$) in order to deliver high current per unit width and minimize source/drain resistance (R_{SD}). However, the on-current improvement by increasing N_D reaches a limit because bulk conduction carrier mobility is degraded due to the increased impurity scattering. The device is getting more and more difficult to turn off as N_D increases, because higher gate bias is required to deplete the entire channel. The ultrahigh channel doping concentration will also enhance coupling between drain and channel, which can induce significant drain induced barrier lowering effects (DIBL).[4]

Shrinking the dimension of the fins would help to alleviate the problems; however, the design rules will be tightened. Both the width and thickness of the fins have to be extremely scaled due to the reduced maximum depletion width, W_{DW}, as N_D increases.[5] For example, the fin width needs be as small as 5 nm when $N_D = 8 \times 10^{19}\,cm^{-3}$ for better gate electrostatic control.[6–8] Such a small fin is difficult to fabricate[9] and would deteriorate the conduction current by introducing large parasitic resistance. It may also lead to the swing of threshold voltage due to the potentially larger process variation for smaller scales.[10] The potential threshold swing issue is even worse for JL FETs compared with inversion-mode devices, since JL devices are more sensitive to fin width variability.[11] Introducing non-uniform dopant distribution profiles in the channel is promising, as reported in planar JT devices using a Gaussian doping profile,[12] which showed improvement of the off-current at some expense of the on-current. More systematic design and analysis are needed, especially for JT MuGFETs.

In this letter, we present a design that adopts step-doping scheme in JL MuGFETs, with higher doping concentration on both the top surface as well as the side walls of fins. Comparison with uniform-doping and retrograde-doping reveals that the high-low step-doping is superior in terms of better threshold voltage control, lower off-state leakage, higher on-current with the same total number of dopants, and better short channel effects (SCEs) immunity. We then discuss the underlying mechanism of such improvements and define a scaling factor metric to quantify its improved scalability. The implementation of step-doping could be useful for the scaling of JL MuGFETs.

A JL MuGFET structure employing step-doping profile is schematically shown in Fig. 1. The cross sectional view along A-A′ direction shows the two regions with different doping concentrations, high (N_1, near-surface or shell, shaded with hash lines) and low (N_2, subsurface or core, shaded with grids) as indicated. We will call this the step-doping if it is high to low doped from the surface down; on the contrary, retrograde-doping[13] refers to low to high. For ease of analysis, we assume that the high and low doped regions have the same area A, i.e., $(T_{fin} - T_{td}) \times (W_{fin} - T_{td}) = T_{fin} \times W_{fin}/2$, where T_{fin} and W_{fin} are the total thickness and width of the fin, respectively, and T_{td} is the transition depth. For comparison, we use a control design with the same total number of dopants, but uniformly doped with doping concentration of $(N_1 + N_2)/2$. 3D numerical simulation of the device DC performance was carried out using Synopsis Sentaurus at 300 K. The parameters

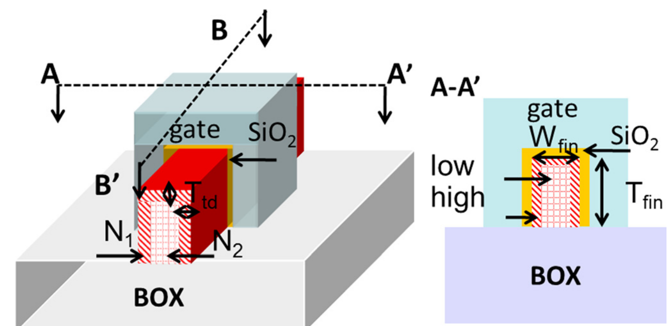

FIG. 1. Schematic of a step doped JL MuGFET structure, The cross sectional view (along A-A′) indicates two different doping regions inside the channel. T_{fin} and W_{fin} are the total thickness and width of the fin, respectively, and T_{td} is the transition depth.

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TABLE I. Summary of structure design parameters for the simulation of JL MuGFETs.

	Uniform	Retrograde-doping	Step-doping
Channel doping (cm^{-3})	2.75×10^{19}	$5 \times 10^{18}/5 \times 10^{19}$	$5 \times 10^{19}/5 \times 10^{18}$
Gate oxide (nm)	2	2	2
Gate workfunction (eV)	5.5	5.5	5.5
Transition depth (T_{td}) (nm)	N/A	2	2
T_{fin} (nm)	20	20	20
W_{fin} (nm)	9	9	9
L_{gate} (nm)	10–170	10–170	10–170
W_{DM} (nm)	7.2	5.5	15

used for simulation of a Si channel are summarized in Table I. Band-to-band tunneling[14] and mobility degradation due to impurity scattering were taken into account.[15] Quantum mechanical correction was not included to save simulation time and should not affect the analysis on different doping schemes. Note that the proposed structure can be readily fabricated either by advanced implantation and annealing technology or by *in situ* doping during epitaxial growth.

Shown in Fig. 2 are the simulated transfer curves I_{ds}-V_{gs} for aforementioned devices ($L_g = 15$ nm) but with three different doping schemes. At $V_{ds} = V_{DD} = 1$ V and $V_{gs} = V_{th} + 2/3V_{DD}$, I_{on} is found to be 650, 480, and 370 μA/μm for step doping, uniform doping, and retrograde doping, respectively, normalized by the fin height. This can be understood because I_{on} can be estimated from the following equation:

$$I_{on} \approx \sum q\mu N \frac{T_{fin}W_{fin}}{L_g} V_{DD}, \qquad (1)$$

where μ is the mobility, N is the carrier concentration, L_g is the gate length, V_{DD} is the supply voltage, and Σ accounts for the summation of the conducting carriers with different μ. Although the total amount of conducting charges in the channels is the same for three designs, the different dopant distribution changes the effective fin width. For the step-doping case, the gate bias converts the channel from depletion to flat band, then to accumulation mode faster because of a smaller effective fin width which will be discussed further later. This leads to more carriers for the same amount of gate voltage overdrive. On the other hand, the mobility difference between the highly doped areas (2.75×10^{19} and $5 \times 10^{19}\,cm^{-3}$) is not significant,[16] while the mobility in the lower doped area ($5 \times 10^{18}\,cm^{-3}$) is much higher which contributes to more current. Therefore, a higher on-current in the step doping scheme is expected.

Furthermore, the sub-threshold behaviors show significant improvement. The subthreshold slope (SS) is lowered to 88 mV/dec for the step-doping scheme from 98 mV/dec for the uniform doping scheme, with the retrograde-doping scheme being the worst at 107 mV/dec. Correspondingly, the step-doping scheme has the lowest off-state current compared with the other two.

The source barrier, which is the maximum difference of the off-state conduction band minimum E_c in the source/channel region, determines the off-state current. Fig. 3 plots the off-state $E_c(x)$ at the interface of Si and SiO_2 along the middle of the fin channel (i.e., along B-B′ in Fig. 1). Both the height and the width of source barrier are slightly larger for the step-doping scheme compared with the other two. Although the difference is small, it may still block the tunneling at off-state more effectively, contribute to lower leakage current.

In addition, the threshold voltage (V_{th}) becomes more and more negative, from step, uniform, to retrograde-doping structures, as can be seen from Fig. 2. This could be attributed to the slope of electric field (dE/dx) in the channel. The lower doped region is located away from the gate metal in the step-doping case, resulting in a reduced dE/dx thus smaller surface potential φ_s[17] compared with the other two. Therefore, lower V_{th} value can be achieved according to Gauss' law (note that the total charge is identical for all cases). This feature is useful for the scalability of JL transistors because it can help turn off transistors without the need of excessively high gate workfunction or scaled fin dimensions.

Fig. 4 examines the SCEs by plotting the V_{th} roll-off as a function of gate lengths (L_g). The steep decay of V_{th} for small L_g can be seen for all doping schemes, but the decay rate is the slowest for the step-doping structure. The trends of SS and DIBL as a function of L_g are also examined and shown in Fig. 5. The step-doping structure shows the lowest SS and DIBL across the entire L_g range. Clearly, the step-doping scheme leads to better SCE immunity.

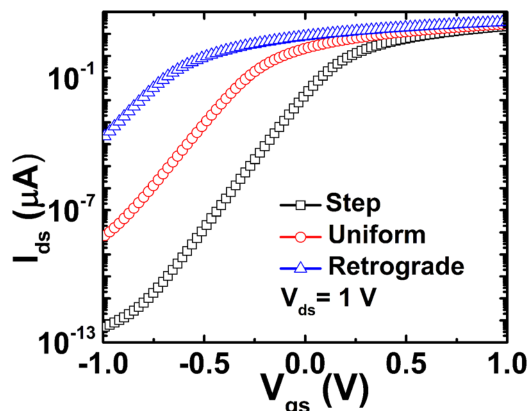

FIG. 2. Comparison of the transfer I_{ds}-V_{gs} curves for different doping schemes with $L_g = 15$ nm and the detailed parameters adopted from Table I.

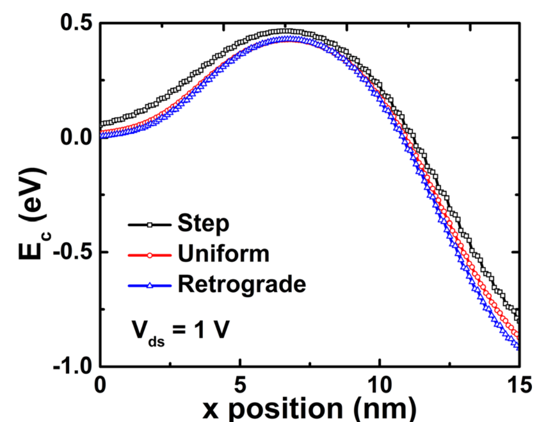

FIG. 3. Comparison of conduction band minimum E_c versus positions in the channel (along B-B′ in Fig. 1) at off-state ($V_{gs} = V_{th} - 1/3*V_{DD}$), for different doping schemes with $L_g = 15$ nm that source at zero and drain at 15 nm in x-axis. The detailed device parameters are adopted from Table I.

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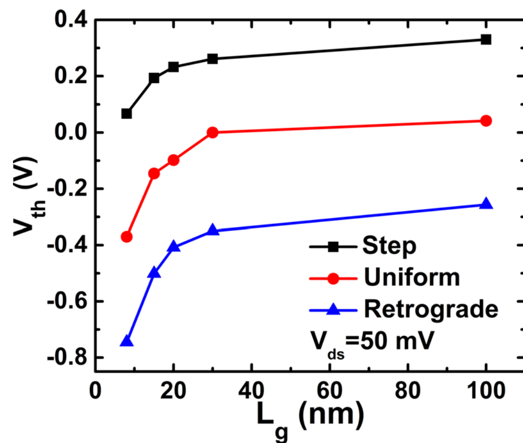

FIG. 4. Comparison of threshold voltage (V_{th}) roll-off with the scaling of the gate length (L_g) between the three different doping schemes.

We believe that the improved SCE immunity results from the smaller effective fin width "seen" by the gate electrode in step-doping and better gate electrostatic control. On one hand, the thicker W_{fin} is, the larger current it can deliver per fin. The maximum W_{fin} is, however, limited by the maximum depletion width W_{DM} in order to ensure total depletion at off-state. On the other hand, lower channel doping concentration, i.e., larger W_{DM}, is desired in order to improve SS, DIBL, and lower leakage for the same W_{fin}.[4] To evaluate the extent of depletion in the channel, we define an effective fin width scale factor $\alpha = W_{fin}/W_{DM}$. The smaller α, the easier the channel can be turned off by complete depletion, which means stronger gate electrostatic control and better SCE immunity.

We compare α for the three doping schemes (1) $N_1 > N_2$; (2) $N_1 = N_2$; and (3) $N_1 < N_2$, where N_1 and N_2 are the near-surface and subsurface doping concentrations, respectively, as indicated in Fig. 1. We assume that (1) and (3) have the same transition depth T_{td} for comparison and $T_{td} < W_{DM,N1}$. By integrating Poison's equation along the normal direction of oxide/Si interface,[5] we can calculate the effective W_{DM} for an arbitrary two-step-doping scheme

$$W_{DM,non-uniform} = \sqrt{T_{td}^2 - \frac{N_1}{N_2} T_{td}^2 + \frac{2\varepsilon_{si}}{qN_2}\varphi_s}, \quad (2)$$

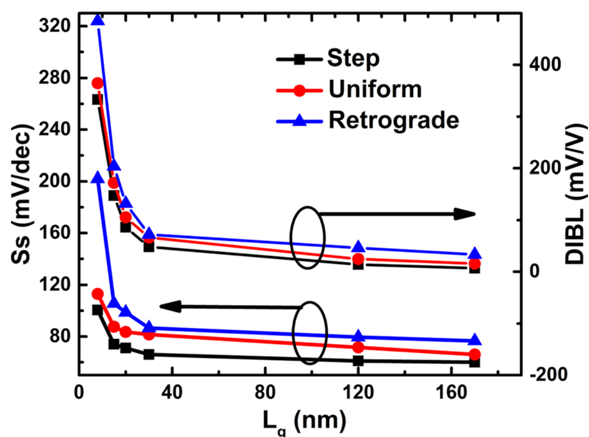

FIG. 5. Subthreshold slop (Ss) and Drain Induced Barrier Lowering (DIBL) comparison verse gate length using the same parameters in Table I.

where $\varphi_s = \frac{kT}{q}(\ln\frac{N_1}{n_i} + \ln\frac{N_2}{n_i})$.

We substituted $N = (N_1 + N_2)/2$ in (2) to obtain the value of $W_{DM,2}$ for the uniform-doping scheme. We found that $W_{DM,1} > W_{DM,2} > W_{DM,3}$ holds true only when $N_1 > N_2$. The calculated values of W_{DM} are 15, 7.2, and 5.5 nm for step, uniform, and retrograde-doping schemes, respectively, using parameters listed in Table I. Since the physical thicknesses W_{fin} are all identical for these three schemes, we can deduce that $\alpha 1 < \alpha 2 < \alpha 3$. Therefore, the step-doping scheme yields the smallest α thus the best off-state control. This also implies that if the same off-state performance is designed for all three schemes, wider fins for the step-doping scheme can be allowed. As a result, step-doping scheme leads to better scalability, by relaxing device fabrication requirements which also should reduce parasitic resistance.

In this letter, we presented a step-doping scheme for the scaling of JL transistors. Lower $|V_{th}|$, higher I_{on}/I_{off} ratio, and better SCE immunity can be achieved with the high-low step-doping in the channel. The standby power consumption is significantly reduced while achieving higher on-state current. The benefits brought by step-doping are attributed to the reduction of effective fin width. This design methodology relaxes the requirement for fin width scaling in JL MuGFETs, allowing continued scaling of JL transistors.

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